EVERSPIN TECHNOLOGIES

Data Persistence at Speed

STT-MRAM Fundamentals, Challenges, and Applications

Syed M. Alam, PhD
Director of Design Engineering

Webinar - Santa Clara Valley IEEE Magnetics Society
Dec 1, 2020

EVERSPIN TECHNOLOGIES

Acknowledgements

- Colleagues at Everspin Technologies:
  - Technology R&D
  - Design
  - Operations

- Partners for STT-MRAM Manufacturing & Development

Safe Harbor Statement

Forward-Looking Statements

This presentation contains "forward-looking statements" that involve risks, uncertainties and assumptions. If the risks or uncertainties materialize or the assumptions prove incorrect, our results may differ materially from those expressed or implied by such forward-looking statements. All statements other than statements of historical fact could be deemed forward-looking statements, including, but not limited to: any estimates of addressable market size and our ability to capture that market, market trends and market opportunities, customer growth, product availability, technology developments, or other future events; any statements about historical results that may suggest future trends for our business; any statements regarding our plans, strategies or objectives with respect to future operations or business performance; any statements regarding future economic conditions; and any statements of assumptions underlying any of the foregoing. These statements are based on estimates and information available to us at the time of this presentation and are not guarantees of future performance. Actual results could differ materially from our current expectations as a result of many factors, including, but not limited to: market adoption of our products; our limited operating history; our ability to raise capital; our history of losses; our rate of growth; our ability to predict customer demand for our existing and future products; our ability to hire, retain and motivate employees; the effects of competition, including price competition; technological, regulatory and legal developments; and developments in the economy and financial markets.

We assume no obligation, and do not intend, to update these forward-looking statements, except as required by law.

The MRAM Promise

PERSISTENCE

Maintains memory contents without requiring power

PERFORMANCE

SRAM & DRAM-like performance with low latency

ENDURANCE

Superior durability supports memory workloads without sophisticated management

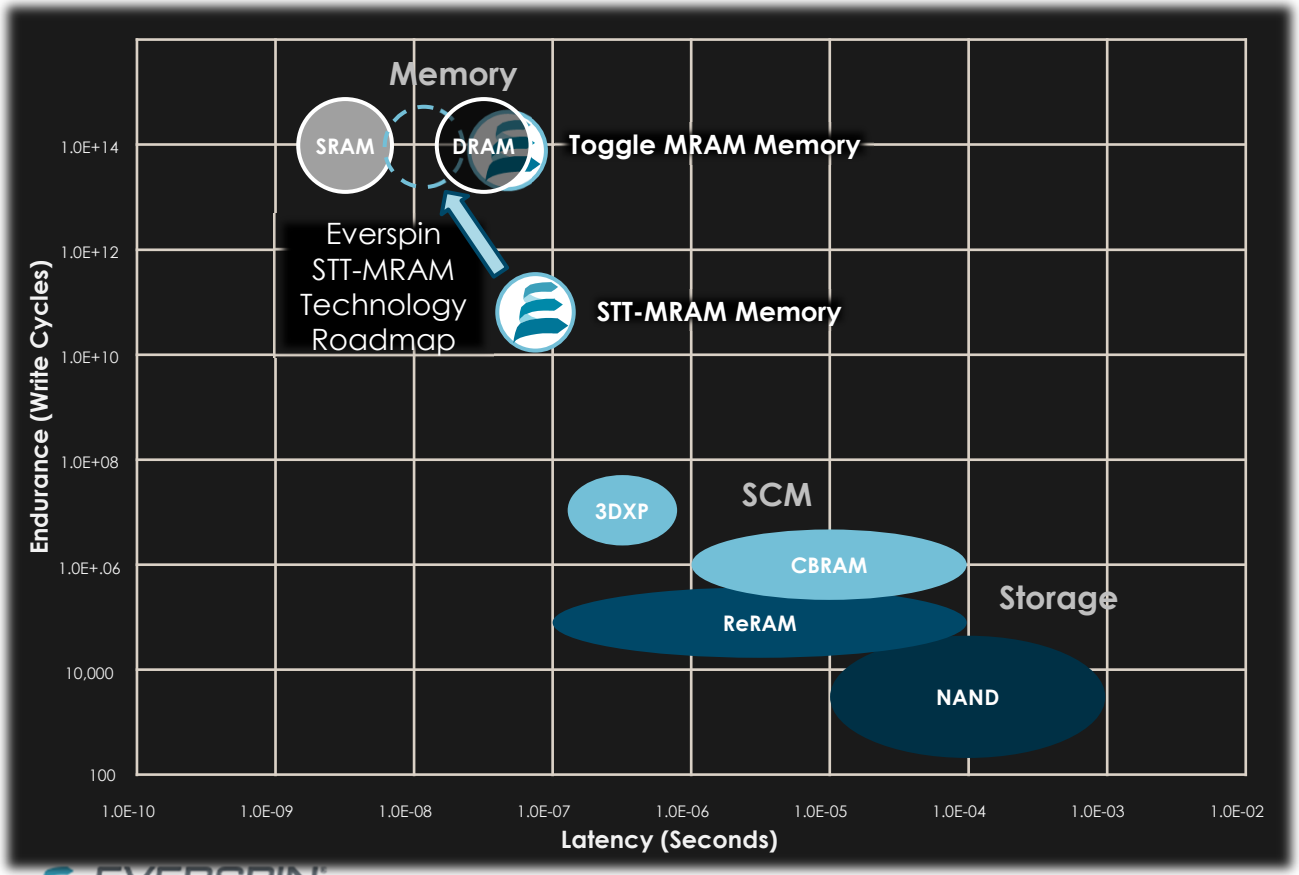
RELIABILITY

Best-in-class robustness designed and tested for extreme conditions

MRAM as a CPU-attached & embedded (like SRAM/DRAM) that brings non-volatility (like Flash)

EVERSPIN TECHNOLOGIES

MRAM Brings Native Persistence to Memory Workloads



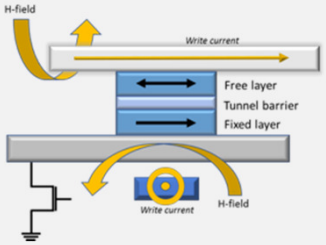
MRAM COMBINES PERFORMANCE OF MEMORY WITH PERSISTENCE OF STORAGE

- **Persistence:** Months to decades of data retention without power or refresh
- **Performance:** Read/write similar to DRAM
- **Endurance:** Handles memory workloads

EVERSPIN TECHNOLOGIES

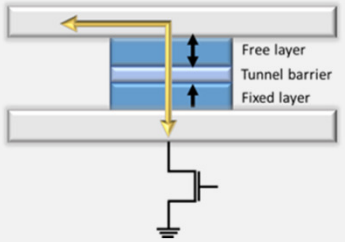
Generations of MRAM

Toggle MRAM as Persistent SRAM



- Standard SPI and Parallel I/F
- Replacement for nvSRAM, FRAM, BBSRAM and NOR Flash
- Robust operating reliability across extended temperature
- Steadily growing long-term market value

STT-MRAM As Persistent DRAM



- DDR3 & DDR4 compatible
- Complementary to DRAM & Flash
- High performance NVM with high chip capacity
- Disruptive value as non-volatile write buffer
- New market growth driver

EVERSPIN TECHNOLOGIES

IBM at FMS 2020: Beating TLC With QLC, MRAM And Computational Storage

4 Comments

+ Add A Comment

by Billy Tallis on November 12, 2020 8:00 AM EST

Posted in SSDs | Storage | Enterprise SSDs | IBM | NVMe | Flash Memory Summit | QLC NAND | Everspin | MRAM

Two years ago we reported on IBM's FlashCore Module, their custom U.2 NVMe SSD for use in their FlashSystem enterprise storage appliances. Earlier this year IBM released the FlashCore Module 2 and this week they detailed it in a keynote presentation at Flash Memory Summit. Like its predecessor, the FCM 2 is a very high-end enterprise SSD with some unusual and surprising design choices.

The most unusual feature of the first IBM FlashCore Module was the fact that it did not use any supercapacitors for power loss protection, nor did the host system include battery backup. Instead, IBM included Everspin's magnetoresistive RAM (MRAM) to provide an inherently non-volatile write cache. The FCM 2 continues to use MRAM, now upgraded from Everspin's 256Mbit ST-DDR3 to their 1Gbit ST-DDR4 memory. The higher-density MRAM makes it much easier to include a useful quantity on the drive, but it's still far too expensive to entirely replace DRAM on the SSD: managing the FCM2's multi-TB capacities require several GB of RAM. IBM's main motivation for using MRAM as a write buffer instead of DRAM with power loss protection is that supercaps or batteries tend to have service lifespans of only a few years, and when an energy storage system fails things can get ugly. IBM sees MRAM as offering better long-term reliability that is worth the cost and complexity of building a drive with three kinds of memory.

In Partnership With:

IBM

imized
eam
gement

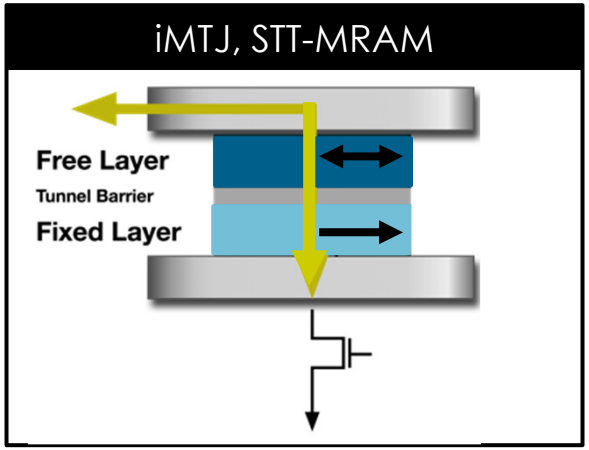
More physical space for storage capacity

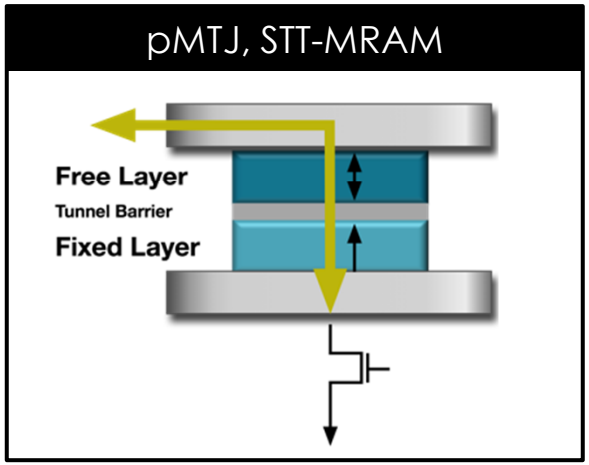
No Capacitor Liability

Simplified Architecture eliminates Power Fail hardening

EVERSPIN TECHNOLOGIES

STT-MRAM Technology



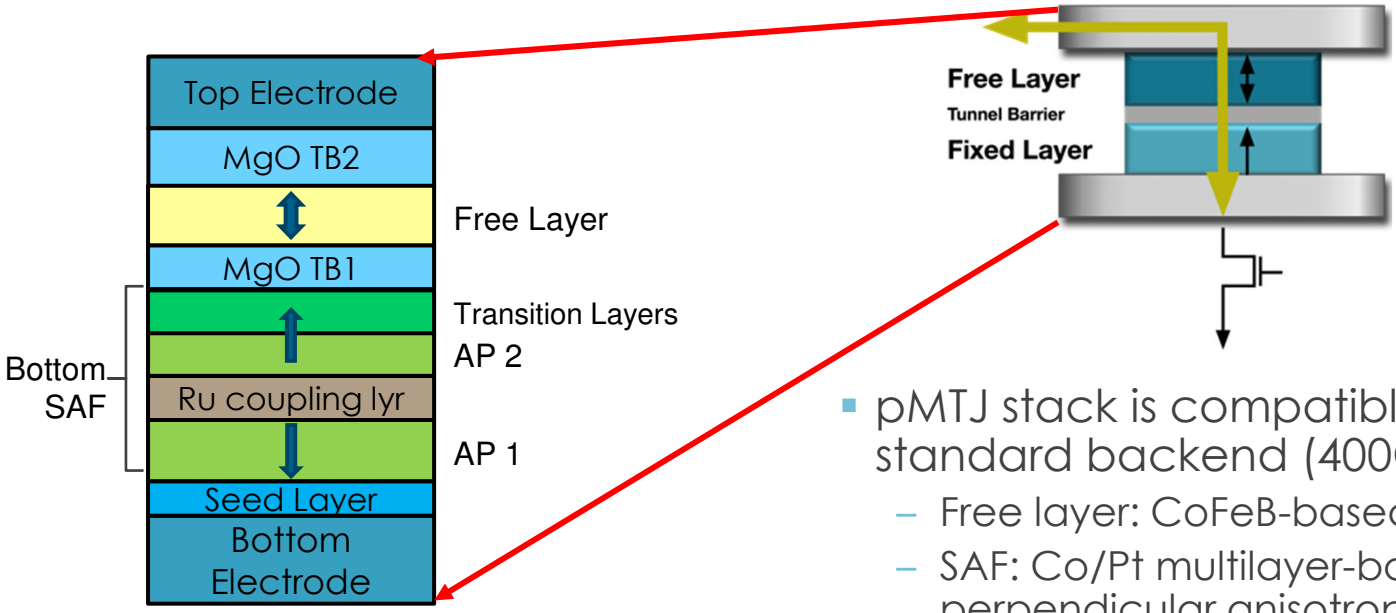


- 64Mb ST-DDR3, 90nm node, i-MTJ developed in Everspin on 8”

- 256Mb ST-DDR3, 40nm node, p-MTJ
- 1Gb ST-DDR4, 28nm node, p-MTJ

EVERSPIN TECHNOLOGIES

Structure of pMTJ device



- pMTJ stack is compatible with standard backend (400C)
  - Free layer: CoFeB-based
  - SAF: Co/Pt multilayer-based for high perpendicular anisotropy

EVERSPIN TECHNOLOGIES

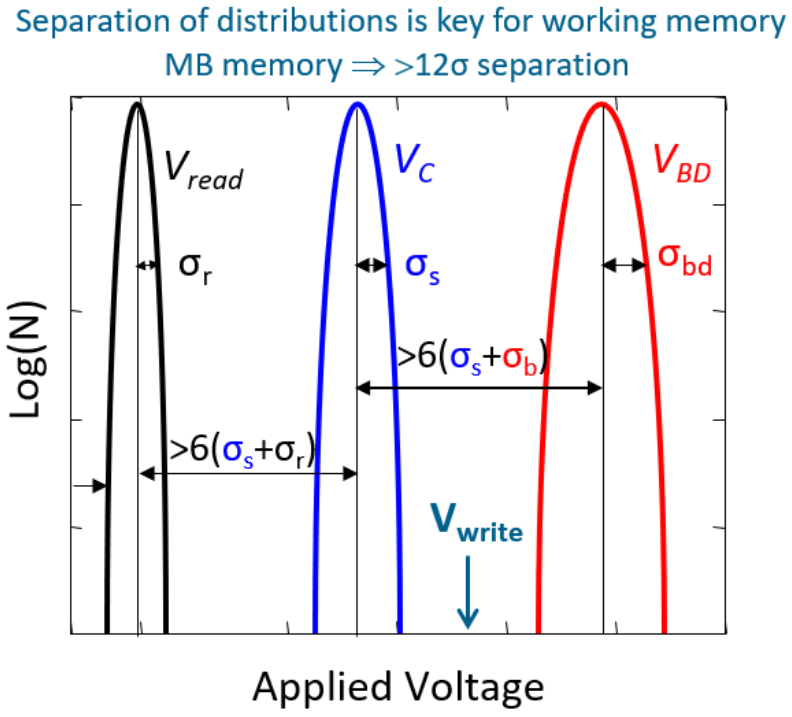
Key requirements for commercial MRAM technology

- Reliable read: High MR and narrow resistance distributions
- Reliable write: Well-behaved switching distributions
- Data retention: High energy barrier (Eb) and narrow distribution
- Cycling endurance:
  - STT-MRAM requires large separation between write and breakdown
    - Low Vc, high Vbd, and narrow, well-behaved distributions for both
- Extrinsic: Very low level of magnetic and electrical extrinsic bits

❖These requirements were met and exceeded to develop pMTJ based products – 256Mb and 1Gb STT-MRAM

EVERSPIN TECHNOLOGIES

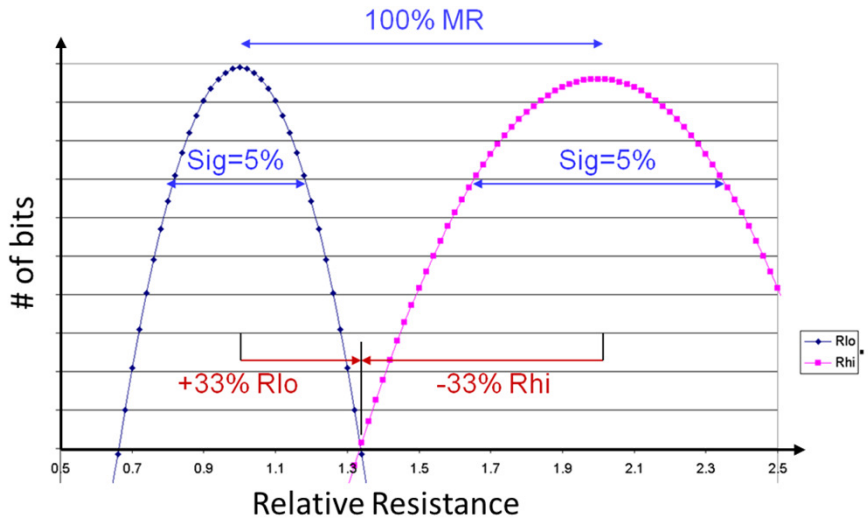
Must separate bit-to-bit distributions in the array



- Separation of V_C & V_{BD}
  - V_{write} must be well above V_C and well below V_{BD}
  - Tight switching distributions
  - Tunnel barrier reliability
- Separation of V_{read} & V_C
  - Avoid read-disturb errors
  - Bigger issue for smaller bits, lower I_C
- Separation gets worse with:
  - Shorter write pulses
  - Smaller bits
  - Extrinsic switching or breakdown behavior

EVERSPIN TECHNOLOGIES

MRAM Read Challenges

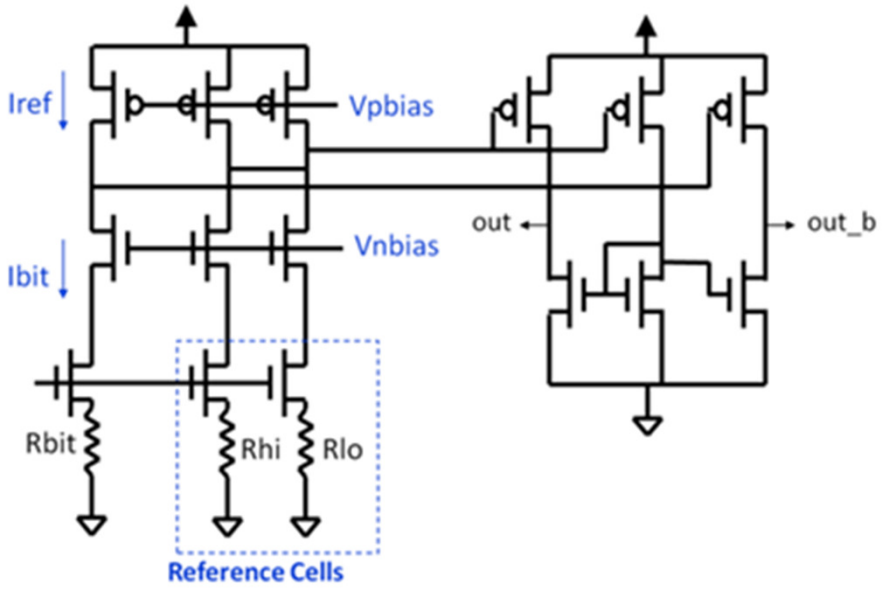


Example Resistance distribution and impact of Rsigma

- State separation requires tight Rsigma
- Midpoint sensing requires signal margin for reference and sense amplifier

EVERSPIN TECHNOLOGIES

Read Sense Amplifier Example

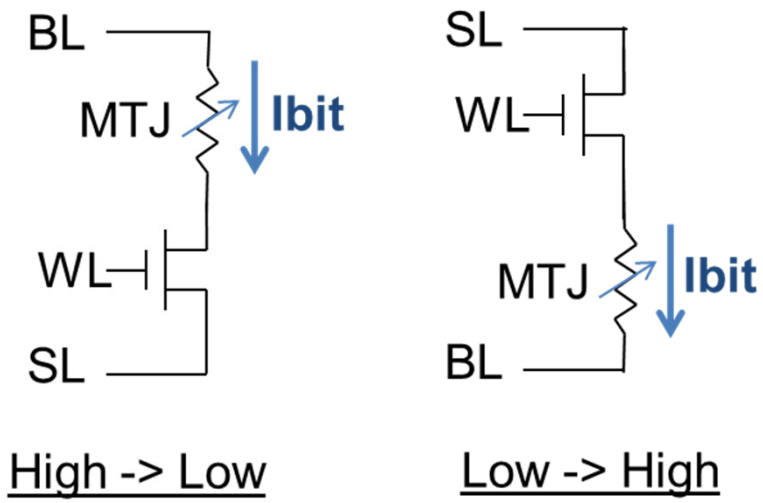


Simplified Midpoint Sensing Example Circuit

- Vnbias source voltage follower controls voltage applied to the bitlines
- Midpoint conductance reference generated by averaging the current for each state

EVERSPIN TECHNOLOGIES

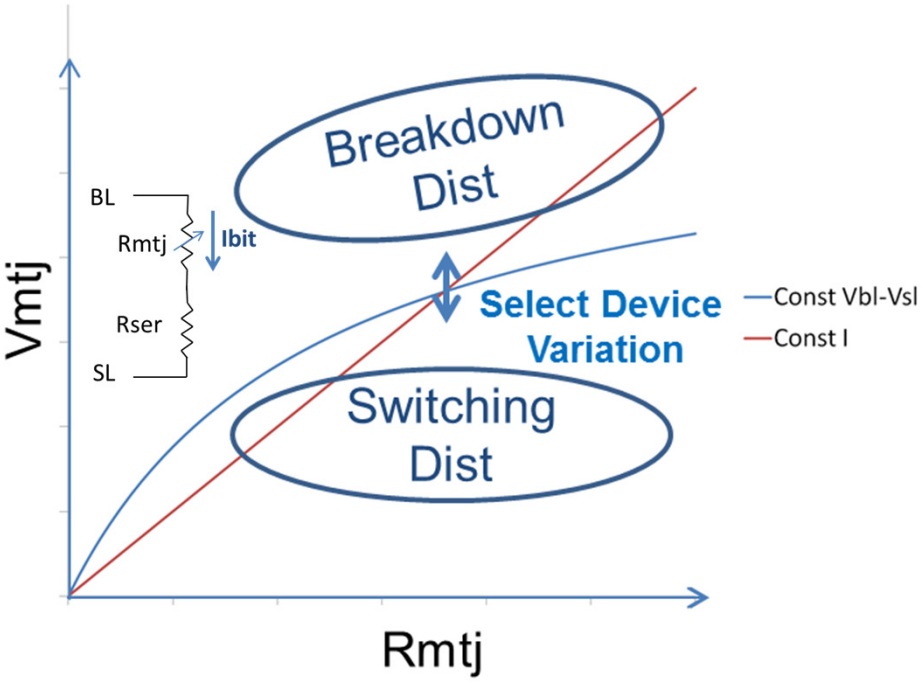
STT-MRAM Writes



- High R -> Low R switching
  - Current flows from BL to SL
- Low R -> High R switching
  - Current flows from SL to BL

EVERSPIN TECHNOLOGIES

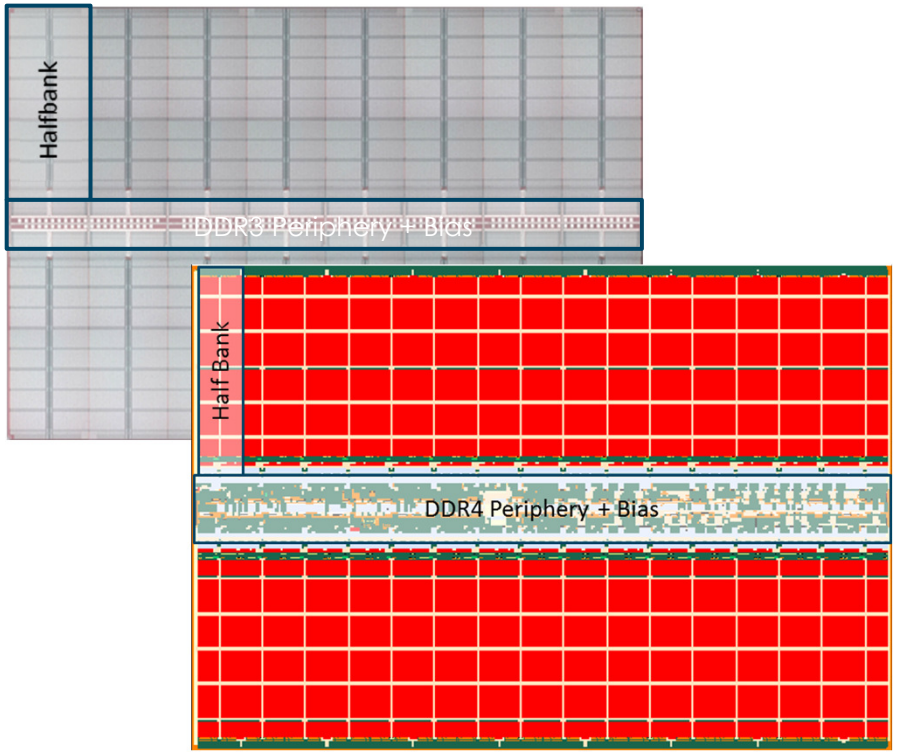
Applied Voltage vs Rmtj



- Constant current eliminates variability from Rser, however, causes large range of Vmtj across the MTJ resistance distribution
- Constant Vbl-Vsl provides applied voltage as a voltage divider between the MTJ and the series resistance

EVERSPIN TECHNOLOGIES

STT-MRAM Product using pMTJ

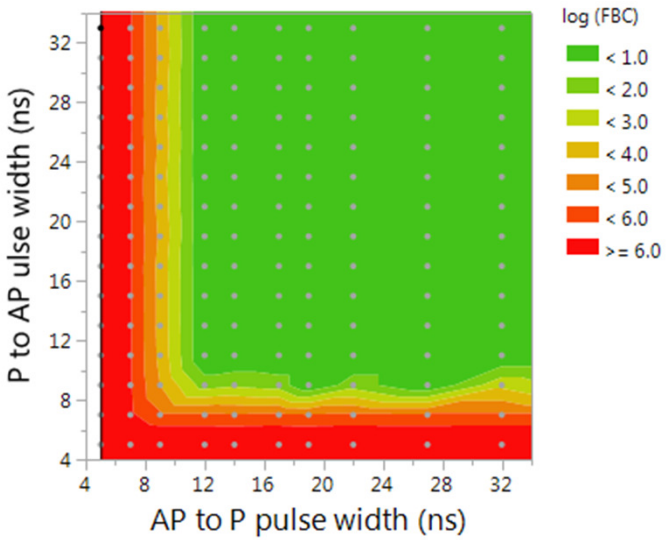


- 256Mb ST-DDR3 MRAM
  - 40nm CMOS
  - 1.5V DDR3 VDD/VDDQ
  - Standard JEDEC DDR3 ball configuration
- 1Gb ST-DDR4 MRAM
  - 28nm CMOS
  - 1.2V standard DDR4 VDD/VPP/VDDQ
  - Standard JEDEC DDR4 ball configuration

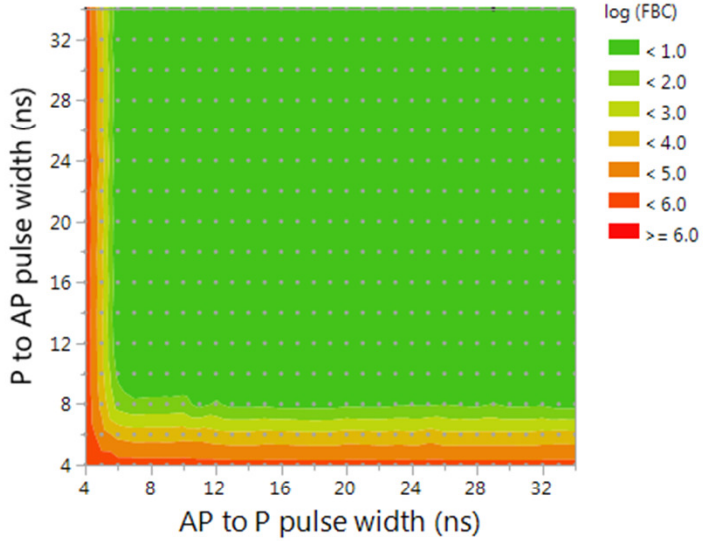
EVERSPIN TECHNOLOGIES

Fast Write Operations

256Mb DDR3 STT-MRAM



1Gb DDR4 STT-MRAM



- Zero fails for range of write pulse widths
  - 256Mb part down to 10-12 ns
  - 1Gb part down to 6-8ns

EVERSPIN TECHNOLOGIES

Summary

- MTJ based MRAM has been in production since 2006
- 1Gb STT-MRAM devices are now in production.
- Read and Write circuit challenges:
  - Read margin requires high MR, tight Rsigma, and a sense amplifier optimized for speed with low mismatch
  - Tight control of BL-SL voltage is required to achieve switching yield while maintaining high endurance
- MTJ optimization design enables customizing STT-MRAM solutions for different applications
- System solutions using STT-MRAM have entered the market

EVERSPIN TECHNOLOGIES

Thank you.

EVERSPIN®
TECHNOLOGIES
Data Persistence at Speed